

Lesson Plan

Name of the Faculty	ABHEY SINGH
Branch	Computer Engineering
Semester	4 th
Subject	Computer Organisation
Lesson Plan Duration	16 Week

WEEK	Theory	
	Lecture Day	Topic (Including Assignment and Test)
1	1 st	Introduction to H/W organization of computer system.
	2 nd	CPU Organization : General Registers organization
	3 rd	Concept of Stack Organization
	4 th	Concept of Instruction Format and types of instruction
2	5 th	Three Address instruction formats
	6 th	Two Address instruction formats
	7 th	One Address instruction formats
	8 th	Zero Address instruction formats
3	9 th	RISC instruction
	10 th	Addressing Modes: Immediate, register, direct
	11 th	Addressing Modes: indirect, relative, indexed
	12 th	CPU Design
4	13 th	Micro programmed controlled
	14 th	Hard wired controlled
	15 th	Revision & problems of unit 1
	16 th	Revision & problems of unit 1
5	17 th	RISC characteristics
	18 th	CISC characteristics
	19 th	CISC & RISC comparison
	20 th	Memory Hierarchy
6	21 st	RAM chip
	22 nd	ROM chip
	23 rd	TEST1
	24 th	Test1 solution
7	25 th	Memory address map
	26 th	Memory connection to CPU

	27 th	Auxiliary memory:
	28 th	Magnetic tapes
8	29 th	Magnetic tapes
	30 th	Associative memory
	31 st	Cache memory
	32 nd	Virtual memory
9	33 rd	Memory management h/w
	34 th	Revision of unit2 & Problems
	35 th	Revision of unit2 & Problems
	36 th	Introduction to BIOS
10	37 th	Function of BIOS
	38 th	Testing and initialization
	39 th	Configure the system
	40 th	Modes of Data Transfer
11	41 st	Programmed I/O
	42 nd	Synchronous data transfer
	43 rd	Asynchronous data transfer
	44 th	Interrupt initiated data transfer
12	45 th	Test2
	46 th	Test2 solution
	47 th	DMA data transfer
	48 th	Revision of unit3 & problems
13	49 th	Revision of unit3 & problems
	50 th	Introduction to multiprocessor system
	51 st	Form of parallel processing
	52 nd	Pipelines
14	53 rd	Pipelines
	54 th	Basic characteristics of multiprocessor
	55 th	General purpose multiprocessor
	56 th	Interconnection networks
15	57 th	Time shared common bus
	58 th	Multi port memory
	59 th	Cross bar switch
	60 th	Multi stage switching networks
16	61 st	Hyper cube structure
	62 nd	Revision of unit 4 & Problems
	63 rd	Revision of unit 4 & Problems
	64 th	Test3

